

<b>Notice of References Cited</b>	Application/Control No. 10/748,557	Applicant(s)/Patent Under Reexamination KOO, KIE-BONG	
	Examiner Tuan T. Nguyen	Art Unit 2824	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-6,424,585 B1	07-2002	Ooishi, Tsukasa	365/226
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	M	US-			

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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	US 2004/0100837 (Jung-Bae Lee) May 27, 2004, On-Die Termination circuit and method for reducing on-chip DC current, and memory system including memory device using the same
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.